

67,200-261; TSMC 99-529/30  
Serial Number 09/821,521

### **REMARKS**

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 9-15 are pending in this application. Claims 9 is amended herein. Claims 1-8 are canceled herein. No claims have been allowed.

#### ***Election/Restriction***

The Examiner has imposed within this application a restriction requirement under which applicant has previously elected prosecution of group II, claims 9-15.

Applicant affirms the foregoing election and also cancels claims 1-8 as directed towards an invention non-elected under the restriction requirement previously imposed within this application.

#### ***Claim Rejections - 35 U.S.C. § 102***

The Examiner has rejected claims 9-15 under 35 U.S.C. § 102(b) as being clearly anticipated by Carroll (U.S. Patent No. 4,657,893).

The Examiner has rejected claims 9-15 under 35 U.S.C. § 102(b) as being clearly anticipated by Eckstein et al. (U.S. Patent No. 5,861,809; hereinafter "Eckstein").

Applicant asserts that applicant's claim 9 is clearly anticipated by neither Carroll nor Eckstein insofar as neither Carroll nor Eckstein discloses a spirally patterned conductor layer which forms a planar spiral inductor having terminated in its center a microelectronic structure which comprises a series of electrically interconnected sub-patterns.

Rather Carroll (cover figure) discloses a spirally patterned conductor layer which forms a planar spiral inductor having terminated in its center a series of logic circuits. Similarly, Eckstein (Fig. 8) discloses a spirally patterned conductor layer which forms a planar spiral inductor having terminated in its center a capacitor plate which is not sub-patterned.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 9 is not disclosed within Carroll or Eckstein, applicant asserts that claim 9 may not properly be rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Carroll or Eckstein.

Since all remaining claims within the foregoing rejections are dependent upon claim 9 and carry all of the limitations of claim 9, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by Carroll or Eckstein.

The Examiner has rejected claims 9-12 and 14-15 under 35 U.S.C. § 102(e) as

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being anticipated by Jacobson et al. (U.S. Patent No. 6,294,401; hereinafter "Jacobson").

Applicant acknowledges the teachings of Jacobson as cited by the Examiner.

In response, applicant has amended claim 9 in a fashion which applicant believes to patentably distinguish applicant's invention as disclosed and claimed within amended claim 9 from that which is disclosed within Jacobson.

In that regard, applicant has amended claim 9 to provide that applicant's microelectronic structure formed within the center of applicant's spirally patterned conductor layer which is formed over applicant's substrate comprises a series of at least four electrically interconnected sub-patterns.

Support for this limitation newly incorporated into amended claim 9 is found within applicant's specification within the last sentence on page 17.

In comparison, Jacobson's microelectronic structure formed within the center of Jacobson's spirally patterned conductor layer comprises only a pair of two electrically interconnected sub-patterns formed over Jacobson's substrate.

Thus, since each and every limitation with respect to applicant's invention as disclosed and claimed within amended claim 9 is not disclosed within Jacobson, applicant asserts that claim 9 may not properly be rejected under 35 U.S.C. § 102(e) as being unpatentable over Jacobson.

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Since all remaining claims within this rejection are dependent upon amended claim 9 and carry all of the limitations of amended claim 9, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(e) as being unpatentable over Jacobson.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 9-12 and 14-15 under 35 U.S.C. § 102(e) as being anticipated by Jacobson be withdrawn.

#### ***Other Considerations***

Applicant acknowledges the prior art of record cited by the Examiner but not employed in rejecting applicant's claims to applicant's invention, including: (1) Staudinger et al. (U.S. Patent No. 5,416,356) and (2) Burghartz et al. (U.S. Patent No. 6,114,937), as generally pertinent to applicant's invention.

No fee is due as a result of this amendment and response.

#### **SUMMARY**

Applicant's invention as disclosed and claimed within amended claim 9 is directed

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towards a microelectronic fabrication, wherein the microelectronic fabrication comprises formed over a substrate a spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer forms a planar spiral inductor, and the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within amended claim 9.

### CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'Randy W. Tung', written over a large, loopy circular flourish.

Randy W. Tung (Reg. No. 31,311)

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**APPENDIX**  
**COMPLETE COPY OF THE CLAIMS**  
**(MARKED-UP WITH CURRENT REVISIONS)**

1. - 8. (canceled)

9. (amended) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns.

10. The microelectronic fabrication of claim 9 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

11. The microelectronic fabrication of claim 9 wherein the microelectronic structure is selected from the group consisting of resistors, diodes, capacitors, bond pads and aggregates thereof.

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12. The microelectronic fabrication of claim 9 wherein the microelectronic structure comprises a capacitor electrically connected with a bond pad.

13. The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

14. The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed in a geometric shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, an ellipse and a circle.

15. The microelectronic fabrication of claim 9 further comprising a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a minimum of one loop.